IN THE CLAIMS

1 (Currently Amended). A method comprising:

forming an analog memory using a phase change material; and

selectively enabling either digital or analog data to be stored in said memory.

Claim 2 (Canceled).

3 (Original). The method of claim 1 including forming a phase change material having a programmably variable resistance for a plurality of cells.

4 (Original). The method of claim 3 including enabling said cells to be addressably located along rows and columns.

5 (Original). The method of claim 1 including forming a phase change material in a pore.

6 (Original). The method of claim 5 including forming a selection device to enable the control of current through said phase change material.

7 (Original). The method of claim 1 including enabling said memory to store in a single cell one of at least three different resistance values.

8 (Original). The method of claim 7 including enabling the resistance of the cell to be set by varying the magnitude of a programming current to the cell.

9 (Original). The method of claim 8 including enabling the resistance of the cell to read and readjust using a different programming current.

10 (Original). The method of claim 9 including enabling a resistance to be set in said cell proportional to a voltage or current characteristic to be stored.

11 (Currently Amended). A memory comprising:

a phase change material; ~~and~~

a circuit to write analog data using said phase change material; and

a circuit to selectively enable either digital or analog data to be stored in said memory.

Claim 12 (Canceled).

13 (Original). The memory of claim 11 wherein said phase change material has a programmably variable resistance.

14 (Original). The memory of claim 13, said memory to store digital and analog data.

15 (Original). The memory of claim 14 wherein said memory to selectively store digital or analog data.

16 (Original). The memory of claim 15 including a circuit to enable a user to select analog or digital data storage.

17 (Original). The memory of claim 16 including an analog read sense amplifier, a digital read sense amplifier, an analog write circuit, and a digital write circuit.

18 (Original). The memory of claim 11 including a substrate, an insulator formed over said substrate, a pore defined in said insulator, and a phase change material in said pore.

19 (Original). The memory of claim 11 including a plurality of cells including a phase change material, said memory including a plurality of conductive lines to selectively enable access to said cells.

20 (Original). The memory of claim 19 wherein said phase change material includes a chalcogenide.

21 (Currently Amended). A system comprising:

a processor;

a wireless interface coupled to said processor; ~~and~~

a semiconductor memory coupled to said processor, said memory including a phase change material, ~~and~~ a circuit to write analog data for storage using said phase change material, and a circuit to selectively enable either digital or analog data to be stored in said memory.

Claim 22 (Canceled).

23 (Original). The system of claim 21, said memory to store digital and analog data.

24 (Original). The system of claim 23 wherein said memory to selectively store digital or analog data.

25 (Original). The system of claim 24 including a circuit to enable a user to select analog or digital data storage.